



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,239	06/24/2003	Rong Yin	02-C-085	5620
7590	12/29/2004		EXAMINER	
Lisa K. Jorgenson, Esq. STMicroelectronics, Inc. 1310 Electronics Drive Carrollton, TX 75006-5039			SHINGLETON, MICHAEL B	
			ART UNIT	PAPER NUMBER
			2817	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Ak

Office Action Summary	Application No.	Applicant(s)
	10/603,239	YIN ET AL.
	Examiner	Art Unit
	Michael B. Shingleton	2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 9/26/04

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) 1-21 and 23-31 is/are allowed.

6) Claim(s) 22 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 22 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Davis, Jr. 5,539,323 (Davis).

Figure 3 of Davis discloses an apparatus having a first circuit composed of elements like element 12 that generates an output signal. Figure 3 of Davis also clearly illustrates a second circuit composed of at least element 15 that is coupled to the output signal of the first circuit. The second circuit detects whether the output signal of the first circuit oscillates at a frequency that is less than a predetermined frequency by the voltage output thereof (See column 3, around line 30). In other words a frequency that is less than a predetermined frequency will correspond to a certain voltage level and accordingly this voltage indicates whether the output signal of the first circuit oscillates at a frequency that is less than a predetermined frequency. The newly amended claim language “by determining whether the output signal remains in one of a first or second logic state in excess of a predetermined period of time” is met by Davis for the same reasons as above and the following: Note that this passage does not limit the output signal to just two logic states. Clearly, one voltage level in Davis would correspond to a first logic state and another voltage level would correspond to a second logic state. Davis utilizes a voltage meter to display the voltage from the frequency to voltage converter 15. Thus, since Davis utilizes real world elements it takes a certain amount of predetermined time to have the circuitry form the logic state and to display and accordingly determines whether the output signal remains in either the first or second logic state in excess of a predetermined time. In other words the time period could be so short where the output signal remains in a first logic state that the circuitry of Davis would and could not display the results. The time period could be so short that the logic state could not be formed. There must be a time in excess of a predetermined time period so that the device of Davis can detect the frequency. The examiner must give the broadest reasonable interpretation to the claim consistent with the specification See MPEP 904.01:

904.01 Analysis of Claims

The breadth of the claims in the application should always be carefully noted; that is, the examiner should be fully aware of what the claims do not call for, as well as what they do require. During patent examination, the claims are given the broadest reasonable

interpretation consistent with the specification. See *In re Morris*, 127 F.3d 1048, 44 USPQ2d 1023 (Fed. Cir. 1997). See MPEP § 2111 - § 2116.01 for case law pertinent to claim analysis.

Allowable Subject Matter

Claims 1-21 and 23-31 are allowed.

Applicant's arguments filed 9-20-2004 have been fully considered but they are not persuasive. Applicant believes that Davis does not operate to make a first or second logic time comparison. The examiner respectfully disagrees. The claim recites detecting and determining which given the broadest reasonable interpretation does not mean that a comparator must be present. The claim is just not so limited as applicant suggests. Note also that a "predetermined" amount can mean any amount.

Accordingly, as noted above this time is set by the speed of the circuits of Davis. If the output is at a first logic state for less than a predetermined period of time or if the output is at a second logic state for less than a predetermined period of time then the device has not detected whether the output signal of the first circuit oscillates at a frequency that is less than a predetermined frequency. If the output is in a first logic state for a period greater than a predetermined period of time and that first logic state corresponds to a frequency less than a predetermined frequency then Davis has detected whether the output signal of the first circuit oscillates at a frequency that is less than a predetermined frequency. Likewise, if the output is in a second logic state for a period greater than a predetermined period of time and that second logic state corresponds to a frequency greater than a predetermined frequency then Davis has detected whether the output signal of the first circuit oscillates at a frequency that is less than a predetermined frequency. In fact in the second case Davis has detected that the output signal is not less than a predetermined frequency. Note that the second logic state could also correspond to a frequency less than a predetermined frequency and the first logic state could also correspond to a frequency greater than a predetermined frequency.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2817

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Tues-Fri from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has second Mondays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS
June 7, 2004
December 23, 2004

Michael B. Shingleton
MICHAEL B. SHINGLETON
PATENT EXAMINER
GROUP ART UNIT 2817